High Rate Digital Demodulator ASIC

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ABSTRACT

The architecture of High Rate (600 Mega-bits per second) Digital Demodulator (HRDD) ASIC capable of demodulating BPSK and QPSK modulated data is presented in this paper. The advantages of all-digital processing include increased flexibility and reliability with reduced reproduction costs. Conventional serial digital processing would require high processing rates necessitating a hardware implementation in other than CMOS technology such as Gallium Arsenide (GaAs) which has high cost and power requirements. It is more desirable to use CMOS technology with its lower power requirements and higher gate density. However, digital demodulation of high data rates in CMOS requires parallel algorithms to process the sampled data at a rate lower than the data rate. The parallel processing algorithms described here were developed jointly by NASA's Goddard Space Flight Center (GSFC) and the Jet Propulsion Laboratory (JPL). The resulting all-digital receiver has the capability to demodulate BPSK, QPSK, OQPSK, and DQPSK at data rates in excess of 300 Mega-bits per second (Mbps) per channel. This paper will provide an overview of the parallel architecture and features of the HRDR ASIC. In addition, this paper will provide an overview of the implementation of the hardware architectures used to create flexibility over conventional high rate analog or hybrid receivers. This flexibility includes a wide range of data rates, modulation schemes, and operating environments. In conclusion it will be shown how this high rate digital demodulator can be used with an off-the-shelf A/D and a flexible analog front end, both of which are numerically computer controlled, to produce a very flexible, low cost high rate digital receiver.

KEY WORDS

Demodulation, binary phase shift keying, quadrature phase shift keying, ASIC

INTRODUCTION

The data rate for NASA missions are increasing very rapidly. In order to process these high data rate high performance processing hardware is required. For baseband data processing, there exists an inexpensive PCI-based solution but for RF processing, the current solutions are based on either all Analog or mixed technology with very little flexibility. For all-digital solution, the Nyquist sampling rate of bandpass data is atleast 2 times the data rate [1]. That is a minimum of 2 samples per symbol are required in order to demodulate the modulated data and then perform carrier recovery, demodulation, and symbol timing recovery with an all-digital receiver. For 210 Megabit data as will be transmitted by the spacecraft EOS-AM1, this is 420 million samples per second. Using conventional serial processing techniques the clock cycle of the digital receiver would have to be 420 MHz. This is high to implement in any current technology and even with higher data rates which are planned for the future, an alternative method to demodulate BPSK/QPSK data needed to be found that would utilize parallel processing. The multirate signal processing algorithms developed by GSFC and JPL to accomplish this require 4 samples per symbol and the demodulator ASIC runs at a clock rate that is one-fourth the data rate. For example, for 210 Mbps data rate, the clock rate required for the HRDD ASIC is 52.5 MHz which can easily be obtained using CMOS technology.

- The HRDD can demodulate BPSK, QPSK, Differential power QPSK, OQPSK, and differential data rate QPSK
- Can demodulate data in the range of 10 Mbps to 300 Mbps
- Bandwidth Range: 500Hz - 10kHz at 10 Msps; 15kHz - 300kHz at 300 Mbps (BW = 0.001 - 0.00005)
- Can compensate for Doppler in the range of +/- 160kHz of Doppler internally with option to be done externally
- The HRDD can demodulate data with SNR as low as 2dB
- Can process Gray encoded data and normal signed and unsigned data
- The implementation loss for the receiver using HRDD ASIC is approximately 1dB off the theoretical curve
- Provides adjustable on the fly phase locked loop filter bandwidths
- Provides programmable lowpass filter coefficients
- Stores internally 8 different loop filter bandwidths but may store loop filter bandwidths externally
- Provides power compensation for Viterbi decoder

HRDD ARCHITECTURE

The design approach for the high rate digital demodulator was algorithm development, software simulations, development of a hardware prototype in reprogrammable hardware, and finally development of a single CMOS ASIC. Figure 1 depicts a block diagram of the of the digital demodulator ASIC.

The input signals to the digital demodulator are 8 parallel 8 bit A/D samples that are demuxed to obtain 16 parallel 8-bit samples. Optionally, these samples can be gray decoded as well as converted from unsigned numbers to signed numbers. Then these 16 samples are digitally mixed with a 10 bit mixer bank in both the I and Q channels and converted to the frequency domain via a modified 32-point DFT. The DFT is modified to eliminate calculating the frequency components of the double frequency term resulting from BPSK/QPSK modulation. The resulting output of the DFT are 15 parallel 13 bit samples. These samples then pass through the lowpass detection filter which filters out the double frequency term followed by the symbol time recovery phase corrector while maintaining 15 parallel 13 bit samples. The coefficients for the lowpass filter are programmable. The data then goes through a modified 32 point IDFT that only outputs the peaks and zero crossings of each symbol with 18 bits resolution. During all of these operations there are always sixteen valid samples being processed in parallel. That is four information bits are being processed simultaneously and four information bits are going out of the IDFT on both the I and Q channel every clock cycle during QPSK demodulation. During BPSK demodulation information bits are going out of the IDFT on the I channel with no information going out on the Q channel. The output of the IDFT is then fed to two digital phase locked loops: symbol time recovery PLL and the Costas PLL. The symbol time recovery PLL is composed of a bit transition detector and a loop

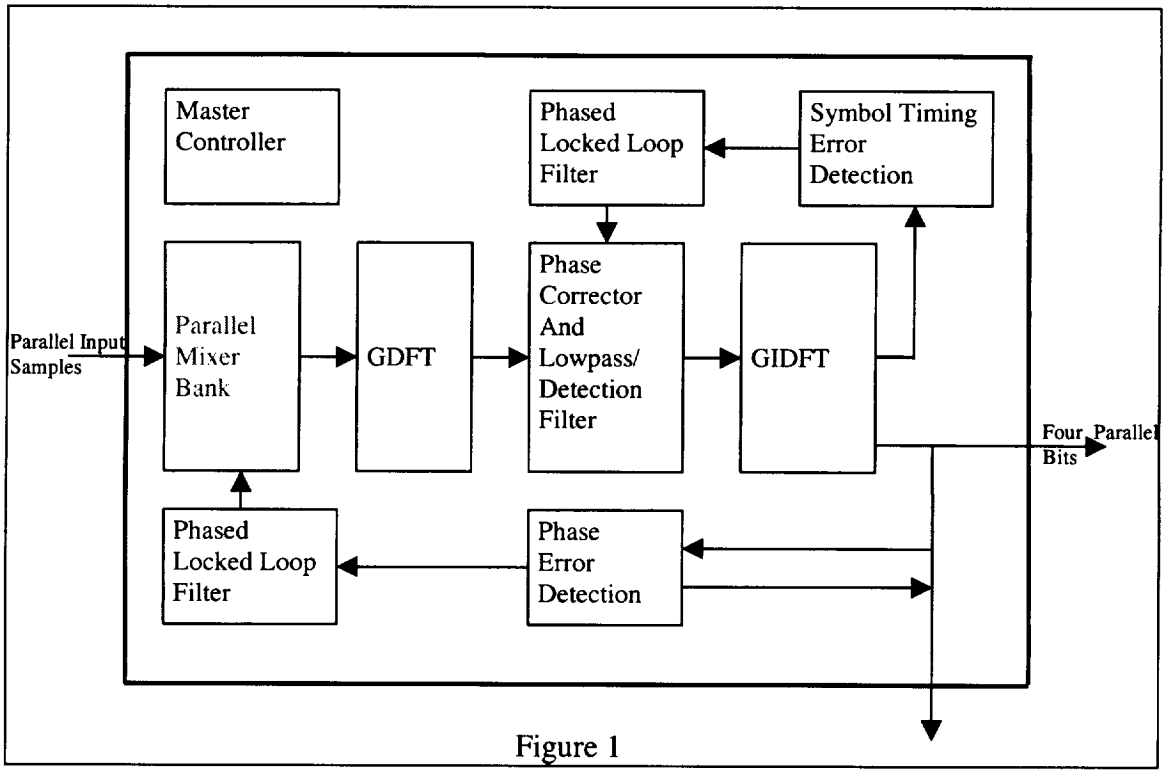

Figure 1

filter that has a resolution of 8 bits that feeds back into the symbol time recovery phase corrector. The Costas PLL is composed of a BPSK/QPSK detection algorithm followed by a loop filter that has a resolution of 10 bits that feeds back into the mixer bank. Up to eight different loop filter coefficients can be loaded in the ASIC along with the option to have the ASIC look up the loop filter coefficients externally. The ouput of the IDFT also passes through the master controller and I and Q channel Power compensator. The master controller's main function is to remove any Doppler on the incoming signal. It does this by determining if the Costas PLL is phase locked and if it is not locked then to introduce a frequency offset in the mixer bank until the Costas loop is phase locked. It does this by averaging the output of the IDFT from the I and Q channel over a set period and comparing the value to a set threshold. If this number is greater than the threshold then the Costas loop is phase lock and if it is less than the threshold the Costas loop is not phase lock. The user also has the capability to select how many times the algorithm will check to verify that it is truly phase locked or not locked to minimize the occurrence of false lock. There is 18 bits resolution given to remove Doppler. The master controller outputs the number of attempts made to remove the Doppler to the user. If the user wanted to develop his/her own frequency acquisition algorithm, then the master controller in the ASIC can be disabled and the output of the IDFT on the I and Q channels can be accessed externally. The I and Q channel power compensator is used only for the differential power QPSK and differential data rate QPSK modes. The power

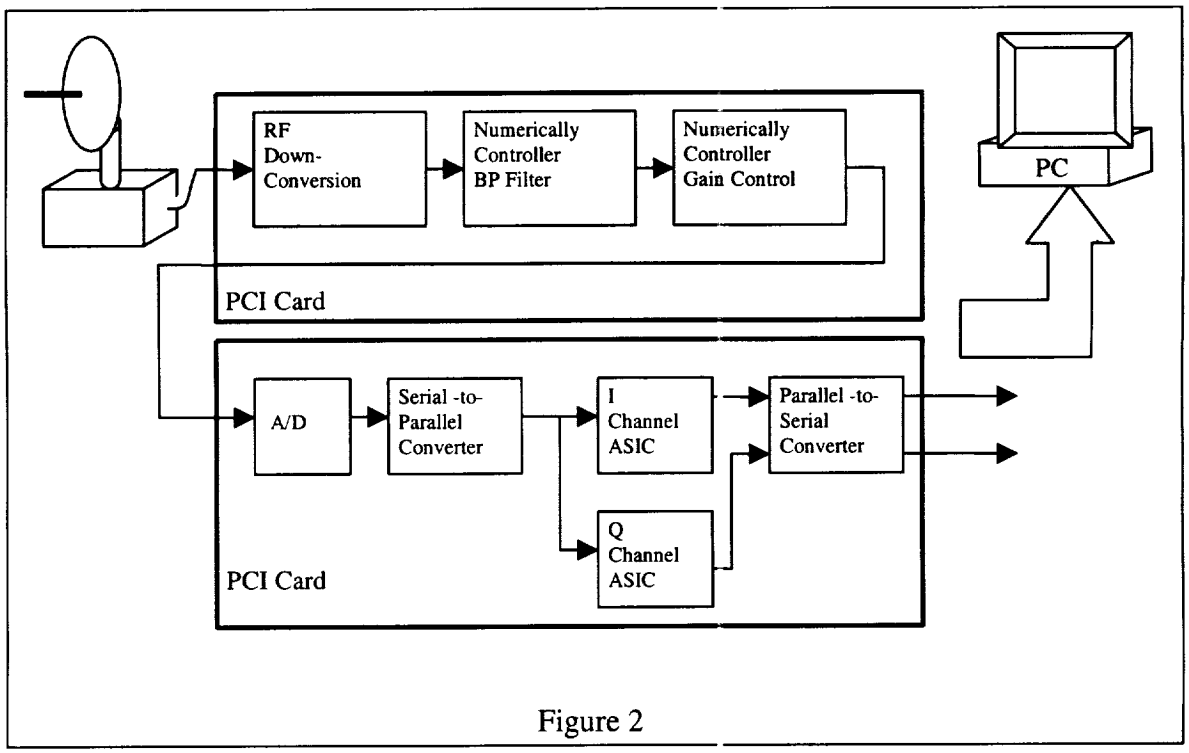

Figure 2

compensator determines which channel, the I or Q, that has the most power and then left shifts the channel with the least amount of power by 2, 4, or 8 depending on the gain of the channel with the most power.

RECEIVER ARCHITECTURE

Figure 2 illustrates the block diagram of the receiver architecture. Two identical HRDD ASICs are used in the digital BPSK/QPSK receiver. One ASIC is the I (in-phase) channel and one the Q (quadrature-phase) channel. Both ASICs, the A/D converter, and supporting digital hardware is designed on a single PCI card. The analog front end is used to mix the data to an appropriate intermediate frequency as well as bandpass filtered prior to the A/D converter. The analog front end is also designed to operate on a single PCI card. The data is sampled four times the data rate and using two 4-bit identical in-house developed GaAs 1-8 demultiplexer, the data is multiplexed and sent to the two HRDD ASICs. These two ASICs performs the demodulation and bit sync operation and send 4 parallel symbols to the next subsystem.

CONCLUSION

This paper has provided an overview of the architecture used to develop a high rate CMOS demodulator ASIC. It has also demonstrated how this ASIC will be used in a digital receiver that provides great improvement in size, cost, and flexibility over currently available high rate BPSK/QPSK receivers.

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